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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/020,113*.

PATENT NO. *9368936*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

FINAL OFFICE ACTION

This Final Office Action addresses the claims 1-56 at issue in ex parte reexamination proceeding No. 90/020,113, involving United States Patent No. 9,368,936 to Lenius et al., entitled LASER DIODE FIRING SYSTEM (hereinafter the "**936 Patent**").

Claims 1-56 are subject to reexamination herein.

Claims 1-31, 33-43 and 45-55 are rejected.

Claims 32, 44 and 56 are patentable.

TABLE OF CONTENTS

I. PRIOR ART REFERENCES AND DOCUMENTS CITED HEREIN

(a) United States Patent No. 7,969,558 to David Hall, issued June 28, 2011 (hereinafter "**Hall**").

(b) United States Patent No. 5,895,984 to Norbert Renz, issued April 20, 1999 (hereinafter "**Renz**").

(c) "GaN Transistors for Efficient Power Conversion," 1st Edition, by Alex Lidow et al., publication date January 20, 2012 and made available to public at least as early as March 2, 2012 (hereinafter "**Lidow**").

(d) "Laser Driver Switching 20A with 2ns Pulse Width Using GaN," May 2010, IEEE MTTS International Microwave Symposium, pp. 1377-1381 (hereinafter "**Liero**").

(e) REBUTTAL EXPERT REPORT OF DR. ANDREW WOLFE, PH.D. CONCERNING THE VALIDITY OF U.S. PATENT NO. 9,368,936, filed under penalty of perjury during the litigation styled Waymo, L.L.C. v. Uber Technologies, Inc., Ottomotto, L.L.C.; Otto Trucking, L.L.C., Case No. 3:17-cv-00939 (U.S. District Court Northern District of California) (hereinafter the "**Wolfe Expert Report**").

(f) EXPERT REPORT OF DR. PHILIP HOBBS ON INVALIDITY OF U.S. PATENT 9,368,936, filed under penalty of perjury during the litigation styled Waymo, L.L.C. v. Uber Technologies, Inc., Ottomotto, L.L.C.; Otto Trucking, L.L.C., Case No. 3:17-cv-00939 (U.S. District Court Northern District of California) (hereinafter the "**Hobbs Expert Report**").

II. RELEVANT PROSECUTION HISTORY

08/01/2017 A request for ex parte reexamination was filed for claims 1-20 of the 936 Patent (hereinafter the "**Request**").

09/15/2017 An order granting ex parte reexamination for all claims 1-20 of the 936 Patent as proposed in the Request was mailed (hereinafter the "**Order**").

12/18/2017 A non-final Office action was mailed rejecting claims 1-20 of the 936 Patent (hereinafter the "**First NF Action**"). The rejections provided therein were based on the Hall, Renz, Lidow and Liero references.

01/30/2018 An interview was held between Examiners and Patent Owner's representatives. An interview summary by the Examiners was mailed February 8, 2018.

02/16/2018 Patent Owner filed a response to the 2018 NF Action, including an amendment adding new claims 21-47 and arguments for patentability for all the claims (hereinafter the "**Feb 2018 Amendment**") and Exhibits A-L. Exhibit C is a declaration by Andrew Wolfe (hereinafter the "**FEB 2018 Wolfe Declaration**").

03/27/2018 A second non-final Office action was mailed rejecting claims 1-28, 30-37 and 49-46 and confirming claims 29, 38 and 47 (hereinafter the "**Second NF Action**"). The rejections were again based on the Hall, Renz, Lidow and Liero references.

05/10/2018 A second interview was held between Examiners and Patent Owner's representatives (hereinafter the "**May 2018 Interview**"). An interview summary was mailed May 18, 2018.

05/29/2018 Patent Owner filed a response to the Second NF Action, including an amendment to the claims and arguments for all of the claims (hereinafter the "**May 2018 Amendment**") and Exhibits A-C. Exhibit A is Applicant's Interview Agenda for the May 2018 Interview. Exhibit B is slides presented by Applicant during the May 2018 Interview. Exhibit C is a supplemental declaration by Andrew Wolfe, Ph.D. (hereafter the "**May 2018 Wolfe Declaration**").

05/31/2018 Patent Owner filed documents in a PTO/SB/08 concerning the litigation styled Waymo, L.L.C. v. Uber Technologies, Inc., Ottomotto, L.L.C.; Otto Trucking, L.L.C., Case No. 3:17-cv-00939 (U.S. District Court Northern District of California).

06/19/2018 A Notice of Defective Paper in Ex Parte Reexamination was mailed.

08/02/2018 A second Notice of Defective Paper in Ex Parte Reexamination was mailed.

08/21/2018 Patent Owner filed a corrected response for the May 2018 Amendment (hereinafter the "**Aug 2018 Correction**"), which corrected the amendment format to the claims and provided an explanation of support for the claim changes.

III. ACKNOWLEDGEMENTS

Examiners acknowledge the May 2018 Amendment and Exhibits A-C filed therewith and further the Aug 2018 Correction. This action is made in full consideration of these documents and all other papers properly made of record herein.

In the May 2018 Amendment and the Aug 2018 Correction, patented claims 1, 9 and 17 were amended, patent claims 2-8, 10-16 and 18-20 were unchanged and new claims 21-56 were added. Of the newly added claims, claims 21 and 26-47 were amended following the Second NF Action and new claims 48-56 have been added. Therefore, claims 1-56 are pending and examined herein. Of these claims, 1, 9 and 17 are independent.

IV. PRIORITY

After review of the prosecution history of the 936 Patent, Examiners find that the 020 Patent was filed as U.S. Application No. 14/132,219, filed December 18, 2013 (hereinafter the "**219 Application**"). The 219 Application claims priority to U.S. Provisional Application No. 61/884,762, filed September 30, 2013 (hereinafter the "**762 Provisional Application**"). Following a review of each of these documents, Examiners find that patent claims 1-20 are entitled to a priority date and effective filing date extending to the filing of the 762 Provisional Application on September 30, 2013.

V. CLAIM INTERPRETATION

(A). Claim Interpretation Overview

After careful review of the original specification, the prosecution history, and unless expressly noted otherwise by the Examiners, the Examiners find that they are unable to locate any lexicographic definitions (either express or implied) with the required clarity, deliberateness, and precision with regard to the patent claims. Patent Owner has not disputed this finding. Because the Examiners are unable to locate any lexicographic definitions with the required clarity, deliberateness, and precision, the Examiners conclude that Applicant is not his own lexicographer for patent claims 1-47. See MPEP §2111.01 IV.

The Examiners further find that because patent claims 1-56 herein recite neither "step for" nor "means for" nor any substitutes therefor, the claims fail Prong (A) as set forth in MPEP §2181(I). Because all examined claims fail Prong (A) as set forth in MPEP §2181(I), the Examiners conclude that all examined claims do not invoke 35 U.S.C. §112(f). See also *Ex parte Miyazaki*, 89 USPQ2d 1207, 1215-16 (B.P.A.I. 2008)(precedential)(where the Board did not invoke 35 U.S.C. §112(f) because "means for" was not recited and because applicant still possessed an opportunity to amend the claims).

Because of the Examiners' findings above that Applicant is not his own lexicographer and patent claims 1-56 do not invoke 35 U.S.C. §112(f), patent claims 1-56 will be given the broadest reasonable interpretation consistent with the specification since patentee has an opportunity to amend claims. See MPEP §2258(I)(G), MPEP

§2111, MPEP §2111.01 and *In re Yamamoto et al.*, 222 USPQ 934 (Fed. Cir. 1984). Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification. See MPEP §2111.01(I). It is further noted it is improper to import claim limitations from the specification, i.e., a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment. See MPEP §2111.01(II).

(B). Specific Interpretations Herein

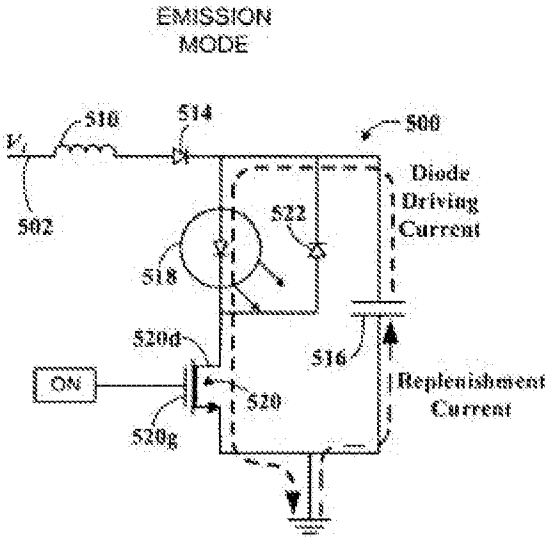
Below are specific interpretations of claim phrases that are not defined in either the claims or the specification, but are necessary to understand the scope of the claims and the manner to which the Examiners consider the prior art applied in the rejections (hereinafter referred to as "**Examiners' interpretation**"). Examiners are not modifying these interpretations as applied in the First NF Action and Second NF Action.

discharge path

As discussed above, Examiners find that the phrase "discharge path" is not lexicographically defined in the specification. Examiners further find that the prior art of record herein does not define this phrase as well. Patent Owner has not disputed this finding. Patent Owner however disputes the interpretation of this phrase as applied in the First NF Action, the Second NF Action and proposed in the Request. Accordingly,

an explanation for the Examiners interpretation of the plain meaning of this phrase is provided below.

As is well known in the art, energy can be stored in the electric fields of a capacitor. See May 2018 Wolfe Declaration ¶45. Specifically, as positive charge builds up on one conductive plate of the capacitor negative charge increases on the other plate. See *Id.* The energy is released by discharging the stored energy. When the capacitor is discharged, there is movement of current around the capacitor, for example movement of charge away from the capacitor on one side thereof and a movement of charge toward the capacitor on the other side. Such movement is shown in the annotated version of FIG. 5D of the 936 Patent, reprinted below, provided by Patent



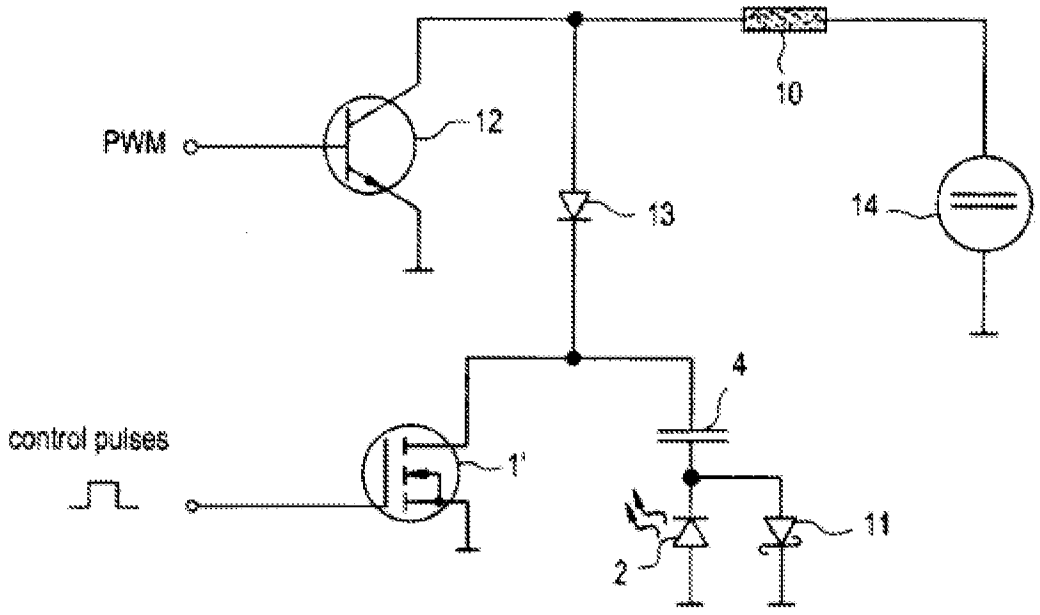
936 Patent FIG. 5D (as annotated by Patent Owner's Expert Andrew Wolfe)

Owner in the May Wolfe Declaration at page 27 and ¶50. See also Feb 2018 Amendment page 9. As shown above, when the capacitor is discharged, a current moves away from the capacitor 516 while current is moving towards it. This is because

the net charge on a capacitor will always be zero. See May 2018 Wolfe Declaration at ¶46.

Thus, in view of these findings and statements by one having ordinary skill in the art, Examiners find that the path of current during the discharge of a capacitor would necessarily include both the path of current moving away from the top plate of the capacitor and the path of current moving towards to the bottom plate of the capacitor. Examiners thus interpret "discharge path" herein as the path of current occurring during the discharge of a capacitor, which would include both of these paths. Such an interpretation is consistent with the explanation of how a capacitor works by Patent Owner's expert.

Furthermore, such a finding is consistent with the disclosure of Renz, which discloses a circuit for charging and discharging a capacitor. For example, Renz states with regard to FIG. 5 of Renz, reprinted below, that when “the MOF-FET in this case



Renz FIG. 5

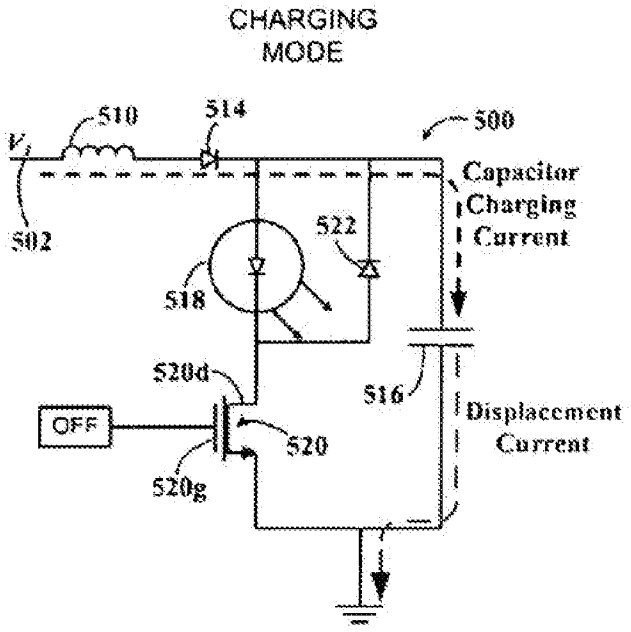
serves to exclusively trigger a useful pulse, that is to say discharge the capacitor 4 through the diode laser." See Renz col. 5, lines 13-15 referring to MOS-FET 1', capacitor 4 and diode laser 2. Specifically, when the MOS-FET is set to "on," the discharge of the capacitor 4 causes current to move away from the capacitor 4 toward the MOS-FET 1' and further current moves towards the capacitor 4 from the ground through the laser diode 2, which causes the laser diode 2 to fire. The laser diode 2 would not fire otherwise. Accordingly, the discharge path necessarily includes the movement of current on both sides of the capacitor, i.e., the path of current moving away from the top plate of the capacitor and the path of current moving toward the bottom plate of the capacitor during discharge. The movement of current along the portion of the discharge path from the ground through the laser diode 2 and the capacitor is the basis for operation of the circuit of Renz to fire the laser diode. The circuit shown in FIG. 23A of Hall discussed below operates in a similar manner.

charging path

As discussed above, Examiners find that the phrase "charging path" is not lexicographically defined in the specification or the prior art of record. Accordingly, along with the explanation above for discharge path, an explanation for the Examiners interpretation is provided below.

As is well known in the art and discussed above, energy can be stored in the electric fields of a capacitor. See May 2018 Wolfe Declaration ¶45. Specifically, as

positive charge builds up on one conductive plate of the capacitor negative charge increases on the other plate. See *Id.* As also discussed above, there is always a net charge is always zero. See Wolfe Declaration ¶46. During charging of the capacitor, a voltage source causes a positive charge to accumulate on one plate of the capacitor and negative charge is accumulated on the other plate. See Wolfe Declaration ¶47. Thus, while the capacitor is being charged, current flows from voltage source to one plate of the capacitor and simultaneously, current flows away from the bottom plate of the capacitor. Such is shown in FIG. 5C of the 936 Patent as annotated by Patent



936 Patent FIG. 5C (as annotated by Patent Owner's Expert Andrew Wolfe)

Owner's expert in on page 25 and ¶¶47-48 of the Wolfe Declaration. See also Feb 2018 Amendment page 9. As shown above, when the capacitor is charged, a current moves towards the top plate of the capacitor 516 while current also moves away from

the bottom plate of the capacitor. This is because the net charge on a capacitor will always be zero.

Thus, in view of these findings and statements by one having ordinary skill in the art, Examiners find that the path of current during the charge of a capacitor would necessarily include both the path of current moving toward the top plate of the capacitor and the path of current away from the bottom plate. Examiners thus interpret "charge path" herein as the path of current occurring during the charging of a capacitor, which would include both of these current paths. Such an interpretation is consistent with the explanation of how a capacitor works by Patent Owner's expert.

(C). Considerations of Patent Owner Arguments Regarding Claim Interpretation

Patent owner traverses the interpretation provided by Examiners above. Specifically, Patent Owner asserts the broadest reasonable interpretation of discharge path is narrower than Examiners' interpretation in that it only includes the discharge path to ground, which is shown as the diode driving current in the annotated FIG. 5D above. See May 2018 Amendment pp. 28-33. Patent Owner's interpretation differs with Examiners' interpretation of discharge path in that is ignores or excludes the portion of the discharge path shown as the replenishment current in the annotated FIG. 5D above. Examiners do not dispute that Patent Owner's interpretation may be reasonable in certain contexts. Examiners simply do not find it is the broadest reasonable interpretation.

Examiners disagree with Patent Owner's arguments as discussed in the responses below. Examiners find that Patent Owner has not shown that the Examiners' interpretation of discharge path is unreasonable.

(1) Patent Owner first argues that the findings by Examiners of how a capacitor works discussed above "does not demonstrate that discharge path is ordinarily and customarily used to refer to both current paths, nor does it demonstrate that such an interpretation is consistent with the specification." See May 2018 Amendment pp. 29. Examiners disagree. First, as noted above, this phrase "discharge path" is not lexicographically defined in any manner in the specification of the 936 Patent. Second, Patent Owner has not disputed that Examiners' findings on how a capacitor works that during discharge of the capacitor, there would be a path of current moving away from the top plate of the capacitor and current moving towards the bottom plate of the capacitor.

Patent Owner is essentially imposing a narrower interpretation that ignores half the current movement along this discharge path. Specifically, Patent Owner would have the Examiners' ignore the movement of current toward the bottom plate of the capacitor during discharge. Such an interpretation is inconsistent with the disclosure of Renz (and Hall FIG. 23A) as discussed above, which during discharge, applies this current towards the bottom plate of the capacitor to fire the laser diodes. Patent Owner's interpretation of discharge path would thus lead Examiners to conclude that circuits of Renz and that of FIG. 23A of Hall would fire their laser diodes without the use of a discharge path. Such an interpretation in untenable and unreasonable in the context of

these references. As stated in Renz, the “MOS-FET in this case serves to exclusively trigger a useful pulse, that is to say discharge the capacitor 4 through the diode laser.” See Renz col. 5, lines 13-15. How would a capacitor discharge through a laser diode but not along a discharge path?? Accordingly, Examiners conclude it would be reasonable to include in the discharge path not only the current moving away from the top plate of the capacitor but also the current moving towards it. Neither current movement would occur without the other on the simple basis of how capacitors work.

Furthermore, Examiners’ interpretation is consistent with the specification. As discussed above, Examiners interpretation of discharge path includes movement of current both away from the capacitor to ground and movement of current from the ground to the capacitor during discharge of the capacitor. Patent Owner's asserted interpretation in view of the specification of discharge path is only that current moving away from the capacitor to the ground. Thus, these interpretations are not inconsistent, but rather one interpretation is merely broader than the other.

Finally, Examiners do not understand how Examiners’ interpretation of discharge path is inconsistent with the specification. As noted above, the specification of the 936 Patent does not lexicographically define discharge path. Furthermore, FIG. 5D of the 936 Patent, identified by Patent Owner as showing the discharge path only illustrates a "diode driving current" or a “current path.” Even in Patent Owner's arguments in distinguishing the prior art, Patent Owners uses "discharge current path." Additionally, the specification of the 936 Patent states the “various example aspects and example embodiments disclosed herein are for purposes of illustration and are not intended to be

limiting." See 936 Patent at col. 27, line 66 to col. 8, line 2. In view of lack of any definition, no examples provided, other phrases used, and the explicit non-limiting specification, Examiners' interpretation of discharge path cannot possibly be inconsistent with any portion of the specification.

In view of the forgoing, Examiners disagree with Patent Owner and do find that Examiners findings with respect to how a capacitor works leads to the logical conclusion that the interpretation of discharge path includes both the current moving towards and away from the capacitor. Examiners find nothing unreasonable about the Examiners' interpretation of discharge path.

(2) Patent Owner also traverses the Examiners interpretation of discharge path on the basis that the Second NF Action "finds fault with the patents submitted as evidence that a POSA would understand the term discharge path to refer to the current path that extends from the top plate of the capacitor and ends at ground." See May 2018 Amendment p. 32. Examiners again disagree and do not find any fault with Examiners' conclusion. First, Examiners note that no reference of record herein or those provided by Patent Owner's expert in the May 2018 Wolfe Declaration (¶50) provides a definition of discharge path. Thus, the plain meaning of discharge path in each of these references must be determined via it usage therein. Furthermore, Examiners note that in each of the references cited in the May 2018 Wolfe Declaration refer to a discharge path "to ground." Patent Owner's arguments also consistently refer to a discharge path "to ground." If the discharge path is so well known, why must each reference clarify where this path leads (i.e., to ground)? Examiners find that in these

statement of the discharge path "to ground" that Patent Owner as well as these references are only interested in or discussing that portion of the discharge path for their discussions, but Examiners find that this simple omission of any discussion of what happens on the other side of the capacitor does not to amount to a limitation of discharge path. If Patent Owner's assertion were accepted, then neither the Patent Owner or any of these references would need to clarify which portion of the discharge path was being referred to (i.e., to ground).

Examiners submit, as in the Examiners interpretation above, the discharge path includes not only a path away from the top plate of the capacitor (to the ground so to speak), but a path towards the bottom plate of the capacitor. The simple fact that these selected references and the 936 Patent omit a discussion of what happens on the other side of the capacitor does not mean the current is not moving along this path during discharge and further does not imply that Examiners' interpretation is unreasonable. At most, these other references and the 936 Patent discussing the discharge path "to ground" provides evidence that they are only concerned with that portion of the discharge path for purposes of their particular circuit.

In view of the forgoing, Examiners' are not attempting to find faults with the references cite in the May 2018 Wolfe Declaration. Rather Examiners are simply concluding that these references do not aid in limiting the plain meaning of discharge path without more as asserted by Patent Owner. Examiners interpretation is consistent with each of the references cited in the May 2018 Wolfe Declaration. Examiners interpretation of discharge path includes both the portion of discharge path from the

capacitor "to ground" and the portion of the discharge path “from ground” to the capacitor. These references merely discuss the former portion of the discharge path as each explicitly identifies the "to ground" discharge path.

(D). Conclusion of Claim Interpretation

As discussed above, Examiners do not find any lexicographic definitions of any claim terms/phrases and no phrases in the claims invoked 35 U.S.C. §112(6th ¶). Accordingly, Examiners will interpret the claims using the broadest reasonable interpretation. Furthermore, in accordance with the broadest reasonable interpretation, Examiners interpret "discharging path" and "charging path" as discussed above.

VI. STATUTORY BASIS FOR ART REJECTIONS

35 U.S.C. §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.
>
> (a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

35 U.S.C. §103(a)

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

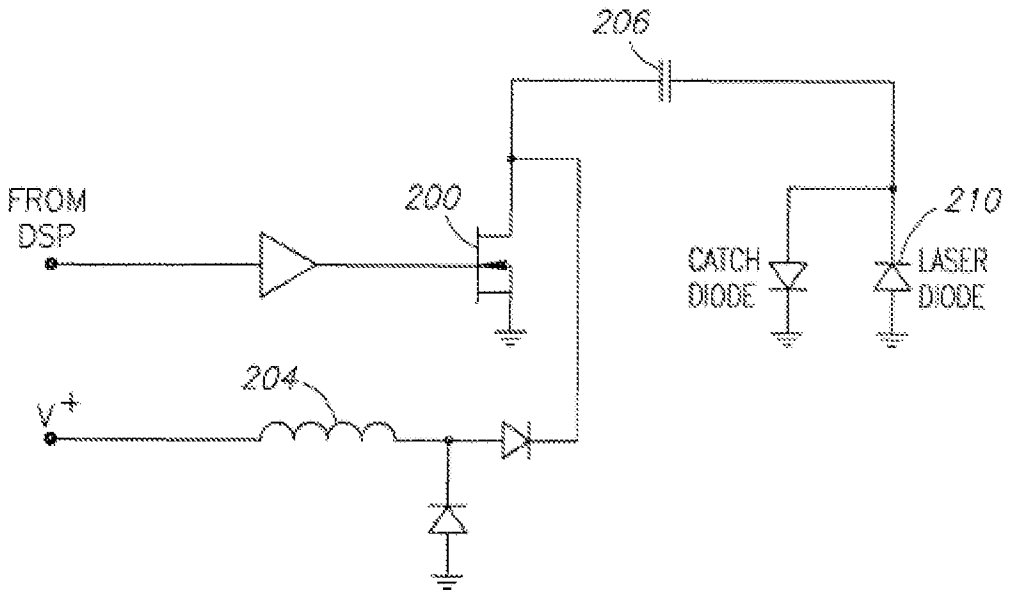
VII. ART REJECTIONS APPLYING EXAMINERS'S CLAIM INTERPRETATION OF CHARGING PATH AND DISCHARGE PATH

The following rejections provided in this section are based on the Examiners' claim interpretation as discussed above in the Claim Interpretation section.

Anticipation Rejections Applying FIG. 23A of Hall

Claims 1-4, 7-15, 17-19, 21, 26-30, 33, 38-42, 45 and 50-54 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by FIG. 23A of Hall. Examiners note Hall is a proper reference for use in this reexamination proceeding because it is a patent. (See MPEP §2210 and §2244--SNQs must be based on patents and printed publications).

Regarding claim 1, FIG. 23A of Hall discloses **an apparatus** (See Hall FIG. 23A, reprinted below)**, comprising:**



Hall FIG. 23A

a voltage source (See FIG. 23A above, note voltage source V+);

an inductor coupled to the voltage source, wherein the inductor is configured to store energy in a magnetic field (See FIG. 23A above, note inductor 204);

a diode coupled to the voltage source via the inductor (See FIG. 23A, note diode shown but not identified coupled to inductor 204);

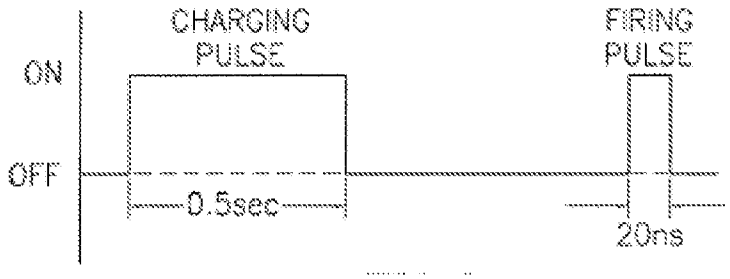
a transistor configured to be turned on and turned off by a control signal (See FIG. 23A, note transistor 200 activated by DSP control signal);

a light emitting element coupled to the transistor (See FIG. 23A above, note laser diode 210);

a capacitor coupled to a charging path and a discharge path (See FIG. 23A, note capacitor 206. Note also Examiners' interpretation of charging path and discharge

path)**, wherein the charging path includes the inductor and the diode, and wherein the discharge path includes the transistor and the light emitting element** (See FIG. 23A above, note charging path would include at least the inductor 204 and shown but not identified diode and discharge path would include at least the transistor 200 and the laser diode 210. See also Hall col. 7, lines 17-41)**;**

wherein, responsive to the transistor being turned off, the capacitor is charges via the charging path such that a voltage across the capacitor increases from a lower voltage level to a higher voltage level and the inductor is configured to release energy stored in the magnetic field such that a current through the inductor decreases from a higher current level to a lower current level (See FIG. 23A above, note configuration shown which provided the recited functionality. See also FIG. 24, reprinted below and col. 7, lines 17-41. Note that in response to the transistor 200 turning off during the .5sec charging pulse, the capacitor 206 charges)**; and**



Hall FIG. 24

wherein, responsive to the transistor being turned on, the capacitor discharges through the discharge path such that the light emitting element emits a pulse of light and the voltage across the capacitor decreases from the higher voltage level to the lower voltage level and the inductor is configured to store

energy in the magnetic field such that the current through the inductor increases from the lower current level to the higher current level (See FIG. 23A, note configuration shown which provided the recited functionality. See also FIG. 24, reprinted below and col. 7, lines 17-41. Note that in response to the transistor 200 turning on during the 20ns firing pulse, the capacitor 206 discharges. Note also that the inductor is "configured" to store energy at this time).

Regarding claim 2, FIG. 23A of Hall discloses the apparatus of claim 1 and further wherein **the lower current level is approximately zero** (See col. 7, lines 27-29 wherein energy stored in the inductor is transferred to the capacitor when the transistor is turned off. Thus, the energy remaining in the inductor is "approximately zero").

Regarding claim 3, FIG. 23A of Hall discloses the apparatus of claim 1 and further wherein **the capacitor is charged immediately following emission of a pulse of light from the light emitting element** (See FIG. 23A and FIG. 24 above, note configuration shown provides the noted functionality. See also col. 7, lines 17-41 wherein following the pulse of light, the transistor 200 is turned off and the energy of the inductor 204 is transferred to the capacitor 206. Note also that the capacitor 206 would begin to charge immediately following the emission of the pulse of light in the gaps between the firing pulse and the charging pulse based on the topography of circuit, i.e., a series circuit of the voltage source V+, the inductor 204, the diode, the capacitor 206, the catch diode and ground when the switch 200 is open).

Regarding claim 4, FIG. 23A of Hall discloses the apparatus of claim 1 and further wherein **the higher voltage level is greater than a voltage of the voltage**

source (See FIG. 23A above, note this is merely a property of the circuit shown)**, and wherein the diode has an anode coupled to the voltage source via the inductor and a cathode coupled to the capacitor, such that the diode is forward biased when the voltage across the capacitor is at the lower voltage level and the diode is reverse biased when the voltage across the capacitor is at the higher voltage level** (See FIG. 23A above, note shown but not identified diode coupled in series with the inductor 204).

Regarding claim 7, FIG. 23A of Hall discloses the apparatus of claim 1 and further wherein **the light emitting element is a laser diode** (See FIG. 23A above, note laser diode 210).

Regarding claim 8, FIG. 23A of Hall disclose the apparatus of claim 7 and further comprising **a drain diode coupled across the laser diode, wherein the drain diode is configured to discharge an internal capacitance of the laser diode through the drain diode when the transistor is off** (See FIG. 23A above, note drain/catch diode 21 coupled with laser diode 210).

Regarding claim 9, FIG. 23A of Hall discloses **a method** (See FIG. 23A and FIG. 24 above and col. 7, lines 17-41)**, comprising:**

turning off a transistor (See col. 7, lines 17-41 wherein a transistor is turned on and off)**, wherein the transistor is coupled to a light emitting element** (See FIG. 23A above, note transistor 200 coupled to laser diode 210)**, wherein both the transistor and the light emitting element are included in a discharge path coupled to a capacitor** (See FIG. 23A above. Note also Examiners' interpretation of discharge path

as discussed above. Thus, note discharge path would include transistor 200, capacitor 206 and laser diode 210)**, wherein the capacitor is also coupled to a charging path including a diode and an inductor, wherein the inductor is configured to store energy in a magnetic field, wherein the diode is coupled to a voltage source via the inductor** (See FIG. 23A above. Note also Examiners' interpretation of charging path as discussed above. Thus, note charge path would include voltage source V+, inductor 204 and series connected shown but not identified diode)**, and wherein, responsive to the transistor being turned off, the capacitor charges via the charging path such that a voltage across the capacitor increases from a lower voltage level to a higher voltage level and the inductor is configured to release energy stored in the magnetic field such that a current through the inductor decreases from a higher current level to a lower current level** (See FIG. 23A, note configuration shown which provided the recited functionality. See also FIG. 24 above and col. 7, lines 17-41. Note that in response to the transistor 200 turning off during the .5sec charging pulse, the capacitor 206 charges)**; and**

turning on the transistor, wherein responsive to the transistor being turned on, the capacitor discharges through the discharge path such that the light emitting element emits a pulse of light and the voltage across the capacitor decreases from the higher voltage level to the lower voltage level and the inductor is configured to store energy in the magnetic field such that the current through the inductor increases from the lower current level to the higher current level (See FIG. 23A, note configuration shown which provided the recited functionality.

See also FIG. 24, reprinted below and col. 7, lines 17-41. Note that in response to the transistor 200 turning on during the 20ns firing pulse, the capacitor 206 discharges. Note also that the inductor is "configured" to store energy at this time).

Regarding claim 10, FIG. 23A of Hall discloses the method of claim 9 and further wherein **the lower current level is approximately zero** (See col. 7, lines 27-29 wherein energy stored in the inductor is transferred to the capacitor when the transistor is turned off. Thus, the energy remaining in the inductor is "approximately zero").

Regarding claim 11, FIG. 23A of Hall discloses the method of claim 9 and further wherein **the capacitor is charged immediately following emission of a pulse of light from the light emitting element** (See FIG. 23A and FIG. 24 above, note configuration shown provides the noted functionality. See also col. 7, lines 17-41 wherein following the pulse of light, the transistor 200 is turned off and the energy of the inductor 204 is transferred to the capacitor 206. Note also that the capacitor 206 would begin to charge immediately following the emission of the pulse of light in the gaps between the firing pulse and the charging pulse based on the topography of circuit, i.e., a series circuit of the voltage source V+, the inductor 204, the diode, the capacitor 206, the catch diode and ground when the switch 200 is open).

Regarding claim 12, FIG. 23A of Hall discloses the method of claim 9 and further wherein **the higher voltage level is greater than a voltage of the voltage source** (See FIG. 23A above, note this is merely a property of the circuit shown)**, and wherein the diode has an anode coupled to the voltage source via the inductor and a cathode coupled to the capacitor, such that the diode is forward biased when the**

voltage across the capacitor is at the lower voltage level and the diode is reverse biased when the voltage across the capacitor is at the higher voltage level (See FIG. 23A above, note shown but not identified diode coupled in series with the inductor 204).

Regarding claim 13, FIG. 23A of Hall discloses the method of claim 9 and further wherein **the charging of the capacitor is carried out in about 500 nanoseconds** (Examiners find that this limitation is merely an intended result or property of the circuit and the turning on and off of the transistor in the method recited in claim 9. Accordingly, this limitation is non-limiting of the claim and thus Hall reads on this claim. Additionally and alternatively, since Hall otherwise discloses the recited circuit and performs the recited method steps, the circuit of Hall would be capable of meeting the intended result).

Regarding claim 14, FIG. 23A of Hall discloses the method of claim 9 and further wherein **the light emitting element is a laser diode** (See FIG. 23A above, note laser diode 210).

Regarding claim 15, FIG. 23A of Hall discloses of the method of claim 14 and further comprising **when the transistor is off, discharging an internal capacitance of the laser diode via a drain diode coupled across the laser diode** (See FIG. 23A, note drain/catch diode coupled with the laser diode 210 which performs the recited functionality).

Regarding claim 17, FIG. 23A of Hall discloses **a light detection and ranging (LIDAR) device** (See FIG. 23A above and FIG. 9A and see col. 3, lines 3-4 and col. 4, lines 41-43) **comprising:**

a light source including:

a voltage source (See FIG. 23A above, note voltage source V+);

an inductor coupled to the voltage source, wherein the inductor is configured to store energy in a magnetic field (See FIG. 23A above, note inductor 204);

a diode coupled to the voltage source via the inductor (See FIG. 23A, note diode shown but not identified coupled to inductor 204);

a transistor configured to be turned on and turned off by a control signal (See FIG. 23A, note transistor 200 activated by DSP control signal);

a light emitting element coupled to the transistor (See FIG. 23A above, note laser diode 210);

a capacitor coupled to a charging path and a discharge path (See FIG. 23A, note capacitor 206. Note Examiners' interpretation above for charging path and discharge path)**, wherein the charging path includes the inductor and the diode, and wherein the discharge path includes the transistor and the light emitting element** (See FIG. 23A above, note charging path which would include inductor 204 and shown but not identified diode and discharge path including the transistor 200 and the laser diode 210. See also Hall col. 7, lines 17-41);

wherein, responsive to the transistor being turned off, the capacitor charges via the charging path such that a voltage across the capacitor increases from a lower voltage level to a higher voltage level and the inductor is configured to release energy stored in the magnetic field such that a current through the inductor decreases from a higher current level to a lower current level (See FIG. 23A, note configuration shown which provided the recited functionality. See also FIG. 24 above and col. 7, lines 17-41. Note that in response to the transistor 200 turning off during the .5sec charging pulse, the capacitor 206 charges)**; and**

wherein, responsive to the transistor being turned on, the capacitor is configured to discharge through the discharge path such that the light emitting element emits a pulse of light and the voltage across the capacitor decreases from the higher voltage level to the lower voltage level and the inductor is configured to store energy in the magnetic field such that the current through the inductor increases from the lower current level to the higher current level (See FIG. 23A, note configuration shown which provided the recited functionality. See also FIG. 24, reprinted below and col. 7, lines 17-41. Note that in response to the transistor 200 turning on during the 20ns firing pulse, the capacitor 206 discharges. Note also that the inductor is "configured" to store energy at this time)**;**

a light sensor configured to detect a reflected light signal comprising light from the emitted light pulse reflected by a reflective object (See col. 3, lines 4-9 and col. 4, lines 21-26 wherein the circuit of FIG. 23A is part of a LIDAR system which uses photo detectors as light sensors as part of the system)**; and**

a controller configured to determine a distance to the reflective object based on the reflected light signal (See col. 4, lines 21-43 which uses a DSP to determine ranging information).

Regarding claim 18, FIG. 23A of Hall discloses the device of claim 17 and further wherein **the lower current level is approximately zero** (See col. 7, lines 27-29 wherein energy stored in the inductor is transferred to the capacitor when the transistor is turned off. Thus, the energy remaining in the inductor is "approximately zero").

Regarding claim 19, FIG. 23A of Hall discloses the device of claim 17 and further wherein **the capacitor is charged immediately following emission of a pulse of light from the light emitting element** (See FIG. 23A and FIG. 24 above, note configuration shown provides the noted functionality. See also col. 7, lines 17-41 wherein following the pulse of light, the transistor 200 is turned off and the energy of the inductor 204 is transferred to the capacitor 206. Note also that the capacitor 206 would begin to charge immediately following the emission of the pulse of light in the gaps between the firing pulse and the charging pulse based on the topography of circuit, i.e., a series circuit of the voltage source V+, the inductor 204, the diode, the capacitor 206, the catch diode and ground when the switch 200 is open).

Regarding claim 21, FIG. 23A of Hall discloses the apparatus of claim 1 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the discharge path forms a current path beginning at the first terminal of the capacitor and ending at ground** (See FIG. 23A above, note capacitor 206 has two terminals. Further note Examiners' interpretation of discharge path would include the

current path flowing away from the top plate of the capacitor 206 and ending at ground and further the current path flowing to the bottom plate of the capacitor 206 from the ground during discharge of the capacitor 206. This finding is in view of the open language of the claim and the Examiners' claim interpretation of discharge path).

Regarding claim 26, FIG. 23A of Hall discloses the apparatus of claim 1 and further wherein **responsive to turning the transistor off, the capacitor charges to a voltage level equal to or greater than a voltage of the voltage source** (See FIG. 23A and FIG. 24 above and col. 7, lines 18-41 wherein following the charging pulse when the transistor 200 is turned off, the energy stored in the inductor 204 is transferred to charge the capacitor 206).

Regarding claim 27, FIG. 23A of Hall discloses the apparatus of claim 1 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the capacitor discharges and charges, respectively** (See FIG. 23A above, note control signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall. Note also in view of the FIGS. 23A and 24, the transistor is turned on and off once and only once each time the capacitor discharges and each time the capacitor charges as shown in FIG. 24).

Regarding claim 28, FIG. 23A of Hall discloses the apparatus of claim 1 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the light emitting element**

emits the pulse of light (See FIG. 23A above, note control signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall. Note also in view of the FIGS. 23A and 24, the transistor is turned on and off once and only once each time the capacitor discharges, i.e., the firing pulse, to cause the light emitting element to emit a pulse of light).

Regarding claim 29, FIG. 23A of Hall discloses the apparatus of claim 1 and further comprising **a gate driver to provide the control signal to turn on and turn off the transistor, wherein the gate driver provides the control signal to one and only one transistor to charge and discharge the capacitor** (See FIG. 23A above, note control signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall, which is connected to only one transistor 200).

Regarding claim 30, FIG. 23A of Hall discloses the apparatus of claim 1 and further wherein **the capacitor charges in response to turning off the transistor and only in response to turning off the transistor** (See FIG. 23A and FIG. 24 above, note capacitor 206 only charges when the transistor 200 is open or turned off).

Regarding claim 33, FIG. 23A of Hall discloses the method of claim 9 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the discharge path forms a current path beginning at the first terminal of the capacitor and ending at ground** (See FIG. 23A above, note capacitor 206 has two terminals. Further note Examiners' interpretation of discharge path would include the current path flowing away from the top plate of the capacitor 206 and ending at ground and further the current path flowing to the bottom plate of the capacitor 206 from the

ground during discharge of the capacitor 206. This finding is in view of the open language of the claim and the Examiners' claim interpretation of discharge path).

Regarding claim 38, FIG. 23A of Hall discloses the method of claim 9 and further wherein **responsive to turning the transistor off, the capacitor charges to a voltage level equal to or greater than a voltage of the voltage source** (See FIG. 23A and FIG. 24 above and col. 7, lines 18-41 wherein following the charging pulse when the transistor 200 is turned off, the energy stored in the inductor 204 is transferred to charge the capacitor 206).

Regarding claim 39, FIG. 23A of Hall discloses the method of claim 9 and further wherein **turning on the transistor and turning off the transistor is performed once and only once each time the capacitor discharges and charges, respectively** (See FIG. 23A above, note control signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall. Note also in view of the FIGS. 23A and 24, the transistor is turned on and off once and only once each time the capacitor discharges and each time the capacitor charges as shown in FIG. 24, respectively).

Regarding claim 40, FIG. 23A of Hall discloses the method of claim 9 and further wherein **turning on the transistor and turning off the transistor is performed once and only once each time the light emitting element emits the pulse of light** (See FIG. 23A above, note control signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall. Note also in view of the FIGS. 23A and 24, the transistor is turned on and off once and only once each time the capacitor discharges, i.e., the firing pulse, to cause the light emitting element to emit a pulse of light).

Regarding claim 41, FIG. 23A of Hall discloses the method of claim 9 and further wherein **one and only transistor is controlled to charge and discharge the capacitor** (See FIG. 23A, note transistor 200).

Regarding claim 42, FIG. 23A of Hall discloses the method of claim 9 and further wherein **the capacitor charges in response to turning off the transistor and only in response to turning off the transistor** (See FIG. 23A and FIG. 24 above, note capacitor 206 only charges when the transistor 200 is open or turned off).

Regarding claim 45, FIG. 23A of Hall discloses the device of claim 17 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the discharge path forms a current path beginning at the first terminal of the capacitor and ending at ground** (See FIG. 23A above, note capacitor 206 has two terminals. Further note Examiners' interpretation of discharge path would include the current path flowing away from the top plate of the capacitor 206 and ending at ground and further the current path flowing to the bottom plate of the capacitor 206 from the ground during discharge of the capacitor 206. This finding is in view of the open language of the claim and the Examiners' claim interpretation of discharge path).

Regarding claim 50, FIG. 23A of Hall discloses the device of claim 17 and further wherein **responsive to turning the transistor off, the capacitor charges to a voltage level equal to or greater than a voltage of the voltage source** (See FIG. 23A and FIG. 24 above and col. 7, lines 18-41 wherein following the charging pulse when the transistor 200 is turned off, the energy stored in the inductor 204 is transferred to charge the capacitor 206).

Regarding claim 51, FIG. 23A of Hall discloses the device of claim 17 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the capacitor discharges and charges, respectively** (See FIG. 23A above, note control signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall. Note also in view of the FIGS. 23A and 24, the transistor is turned on and off once and only once each time the capacitor discharges and each time the capacitor charges as shown in FIG. 24, respectively).

Regarding claim 52, FIG. 23A of Hall discloses the device of claim 17 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the light emitting element emits the pulse of light** (See FIG. 23A above, note control signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall. Note also in view of the FIGS. 23A and 24, the transistor is turned on and off once and only once each time the capacitor discharges, i.e., the firing pulse, to cause the light emitting element to emit a pulse of light).

Regarding claim 53, FIG. 23A of Hall discloses the device of claim 17 and further comprising **a gate driver to provide the control signal to turn on and turn off the transistor, wherein the gate driver provides the control signal to one and only one transistor to charge and discharge the capacitor** (See FIG. 23A above, note control

signals for circuit are provided by a laser driver shown in FIGS. 9A and 9B of Hall, which is connected to only one transistor 200).

Regarding claim 54, FIG. 23A of Hall discloses the device of claim 17 and further wherein **the capacitor charges in response to turning off the transistor and only in response to turning off the transistor** (See FIG. 23A and FIG. 24 above, note capacitor 206 only charges when the transistor 200 is open or turned off).

Obviousness Rejections Applying FIG. 23A of Hall and Liero

Claims 5, 6, 16 and 20 are rejected under 35 U.S.C. 103 as being unpatentable over FIG. 23A of Hall in view of Liero. Examiners find that Liero is proper in this reexamination proceeding because it is a printed publication. (See MPEP §2210 and §2244--SNQs must be based on patents and printed publications). Examiners further find that Liero was published in IEEE as part of the IEEE MTT-S International Symposium in May 2010.

Regarding claim 5, FIG. 23A of Hall teaches the device of claim 1 and further the use of a field effect transistor, but not the specific type thereof. Nevertheless, Liero teaches the use of **gallium nitride field effect transistors (GaNFET)** for various applications. (See Liero Part I, Introduction). It would have been obvious at the time of the effective filing date to use GaNFETs for the transistors in the apparatus of FIG. 23A of Hall. One having ordinary skill in the art would make such a combination to provide a transistor that is an "ideal candidate ... for applications, where fast switching of high current is needed." (See Liero at least Part I, Introduction). Furthermore, the example

of the application where such "fast switching" is needed to which to apply the GaNFET as taught by Liero is a diode laser circuit. (See Liero Parts I, II and IV wherein the GaNFET is used as the switching transistor for the diode laser circuit).

Regarding claim 6, FIG. 23A of Hall and Liero teach the apparatus of claim 5 and further wherein **the control signal applies voltage to a gate of the GaNFET to selectively turn the GaNFET on and off** (Note combination proposed for claim 5. See also Hall FIG. 23A above wherein the control signal is supplied to the gate of the transistor 200 which would be a GaNFET in view of the combination).

Regarding claim 16, FIG. 23A of Hall teaches the method of claim 9 and further wherein **the transistor is turned on and turned off by applying a control signal to a gate of the transistor** (See FIG. 23A above, note control signal to transistor 200), but not specifically the transistor being a GaNFET transistor. Nevertheless, Liero teaches the use of **gallium nitride field effect transistors (GaNFET)** for various applications. (See Liero Part I, Introduction). It would have been obvious at the time of the effective filing date to use GaNFETs for the transistors in the apparatus of FIG. 23A of Hall. One having ordinary skill in the art would make such a combination to provide a transistor that is an "ideal candidate ... for applications, where fast switching of high current is needed." (See Liero at least Part I, Introduction). Furthermore, the example of the application where such "fast switching" is needed to which to apply the GaNFET as taught by Liero is a diode laser circuit. (See Liero Parts I, II and IV wherein the GaNFET is used as the switching transistor for the diode laser circuit).

Regarding claim 20, FIG. 23A of Hall teaches the device of claim 17 and further the use of a field effect transistor, but not the specific type thereof. Nevertheless, Liero teaches the use of **gallium nitride field effect transistors (GaNFET)** for various applications. (See Liero Part I, Introduction). It would have been obvious at the time of the effective filing date to use GaNFETs for the transistors in the apparatus of FIG. 23A of Hall. One having ordinary skill in the art would make such a combination to provide a transistor that is an "ideal candidate ... for applications, where fast switching of high current is needed." (See Liero at least Part I, Introduction). Furthermore, the example of the application where such "fast switching" is needed to which to apply the GaNFET as taught by Liero is a diode laser circuit. (See Liero Parts I, II and IV wherein the GaNFET is used as the switching transistor for the diode laser circuit).

Obviousness Rejections Applying FIG. 23A of Hall

Claim 13 is rejected under 35 U.S.C. §103 as being unpatentable over FIG. 23A of Hall. See MPEP §2112(III-IV) allowing alternative rejections under 35 U.S.C. §102 and §103 when there is a question of inherency of whether a prior art device is capable of meeting an intended result or property of the claim. As discussed above, Examiners find that wherein the charging of the capacitor is carried out in about 500 nanoseconds is merely an intended result or property of the claimed circuit and method. Nevertheless, even if it is assumed FIG. 23A of Hall does not explicitly disclose or teach such a feature, such charging would be obvious to one having ordinary skill in the art.

Examiners first find that FIG. 23A of Hall otherwise discloses each and every feature of claim 13 and further providing a charging pulse to the capacitor of 5000 nanoseconds, but not explicitly a "charging" of the capacitor in about 500 nanoseconds. Nevertheless, modifying or operating FIG. 23A of Hall to have the relative charging time as recited in the claims would be obvious to one having ordinary skill in the art through routine experimentation because where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation and the claimed device is not patentably distinct from the prior art device. See MPEP §2144.05(ii). It would have thus have been obvious to optimize the charging time of the capacitor in FIG. 23A of Hall to be about 500 nanoseconds because such optimization would be routine skill in the art to maximize the performance of the known circuit structures shown in FIG. 23A of Hall, i.e., optimization of the capacitor structure and the timing of the firing of the transistor.

VIII. ART REJECTIONS APPLYING PATENT OWNER'S INTERPRETATION OF DISCHARGE PATH

The following rejections are made in addition to the rejections above. As discussed in the Claim Interpretation section, Examiners have provided an interpretation of discharge path. Nevertheless Patent Owner argues that this discharge path is limited to only the dashed line shown in FIG. 5D of the 936 Patent, reprinted above, and not that portion of the circuit between the bottom plate of the capacitor and the ground. Specifically, Patent Owner's interpretation of discharge path is only that path of charge

from the top plate of the capacitor to the ground. While Examiners do not agree the discharge path is so limiting under the broadest reasonable interpretation, Examiners nevertheless do not find Patent Owner's interpretation unreasonable. Examiners thus find Patent Owner's interpretation of the discharge path would be an alternative but narrower interpretation than the broadest reasonable interpretation, i.e., simply a reasonable interpretation. Thus, the rejections in this section are made using Patent Owner's interpretation of discharge path in addition to the rejections made using the Examiners interpretation as provided above.[1]

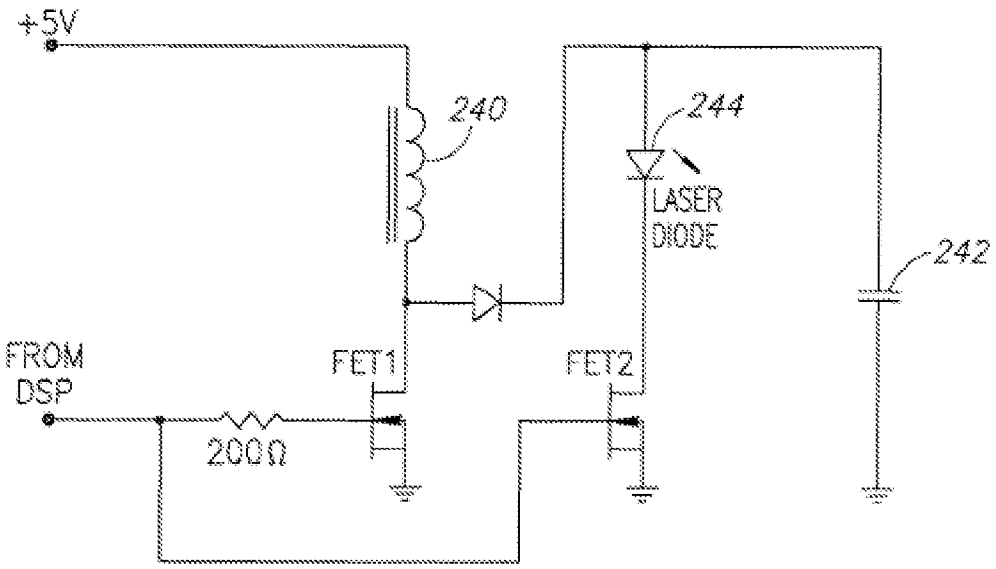
Anticipation Rejections Applying FIG. 23B of Hall

Claims 1-4, 7, 9-14, 17-19, 21-28, 30, 31, 33-40, 42, 43, 45-52, 54 and 55 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by FIG. 23B of Hall. Examiners again note Hall is a proper reference for use in this reexamination proceeding because it is a patent. (See MPEP §2210 and §2244--SNQs must be based on patents and printed publications).

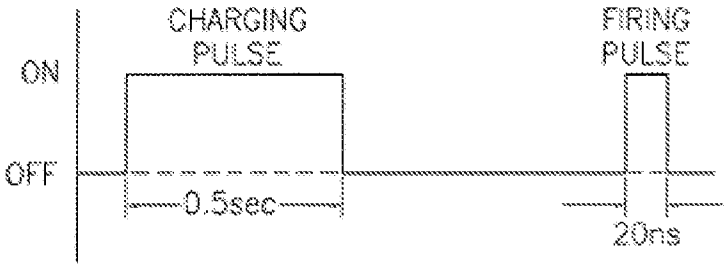
A. Operational Discussion of FIG. 23B of Hall

Before discussing the rejection, Examiners find there is a dispute between the Examiners and Patent Owner regarding the operation of FIG. 23B and FIG. 24 of Hall (reprinted below). This was the primary focus of the interview on May 10, 2018.

[1] Examiners note that since Examiners' Interpretation is a broader interpretation than that proposed by Patent Owner, the rejections in this section would be equally applicable using the Examiners' Interpretation.



Hall FIG. 23B



Hall FIG. 24

During the interview, Patent Owner's representative noted some inconsistency with regard to the operation of FIG. 23B and the activation of the transistors as shown in FIG. 24. See also Wolfe Expert Report ¶¶70-72. Patent Owner's expert Mr. Wolfe also argues that the language used in the Hall Patent is "imprecise." See May 2018 Wolfe Declaration ¶32. Specifically, FIG. 24 and col. 7, lines 42-46 shows and discloses the charging pulse and the firing pulse separately such that during the charging pulse when

FET1 is on, the an inductor 240 charges the capacitor 242 and during the firing pulse when FET2 is on, FET2 causes the capacitor 242 to discharge thereby firing the laser diode 244. Thus, the disclosure and FIG. 24 imply separate control signals for each of FET1 and FET2. However, FIG. 23B shows the DSP providing the same control signals being sent to both FET1 and FET2, with a delay in the control sent to FET1 via the 200Ω resistor. Thus, the inconsistency or impreciseness of operation of Hall is falls into two distinct operations:

(a) FIG. 23B controls and there is simply a delay between the signals sent to FET1 and FET2, or

(b) the specification and FIG. 24 controls and separate control signals are sent to each of FET1 and FET2.

Also during the interview and further elaborated in the May 2018 Amendment, Patent Owner argues that operation (a) is how FIG. 23B of Hall should be interpreted, i.e., the explicit circuit of FIG. 23B controls and the 200Ω resistor merely delays the control signal sent to FET1. Thus, when a charge pulse control signal is sent from the DSP to the transistors, FET2 will turn on first, then FET1 will turn on, then FET2 will turn off, and then FET1 will turn off. See May 2018 Wolfe Declaration ¶¶31-37. There will be a similar delay for the firing pulse. See May 2018 Wolfe Declaration ¶¶31-37. Specifically, at the end of the firing pulse, FET2 will turn off, then there will be a delay before FET2 turns off. Of importance herein, Mr. Wolfe has declared that during this delay between transistors turning off, the closed state of FET1 prevents the capacitor

242 from charging and that only after the FET1 is turned off, the capacitor 242 will begin charging. See May 2018 Wolfe Declaration ¶36.

However, Mr. Wolfe has also declared that operation (b) is also another possible interpretation of the operation of FIG. 23B of Hall. See Wolfe Expert Report ¶73. Mr. Wolfe further states it is "reasonable to interpret the disclosures as indicating that the two transistors FET1 and FET2 operate independently." Id. at ¶74. Specifically, Mr. Wolfe states that both FETs are controlled by the DSP, but "not by the same signal as confirmed by the text." Id at ¶74. Furthermore, Mr. Wolfe declares:

> 75. Assuming FET1 and FET2 operate independently, the charging cycle would begin with FET1 turning on for the duration of the charging pulse to increase current through the inductor, causing it to store energy in a magnetic field. Then FET1 would be turned off causing the energy in the inductor to transfer to the capacitor. Finally, FET2 would be turned on to discharge the capacitor through the laser.
>
> [Wolfe Expert Report ¶75]

Thus, in view of these statement by Patent Owner's expert, in operation (b), the FETs would be operated independently and at different times, i.e., FET1 activated during the charging pulse and FET2 activated during the firing pulse as shown in FIG. 24 above via different control signals. Additionally, neither FET is activated in the period between the firing pulse and the charging pulse. Furthermore, based on the topography of the circuit, "[w]hen FET1 and FET2 of the circuit are off (i.e., the gates of the transistors have no signal applied to them), the circuit is configured to charge the capacitor 242." See Hobbs Expert Report ¶74. Based on these statements as to the operation of FIG. 23B, Examiners find that following, i.e., responsive to, the firing pulse as shown in FIG.

24 after FET1 is turned off, both FETs would be in an off state and the capacitor 242 would charge. See again Hobbs Expert Report ¶74.

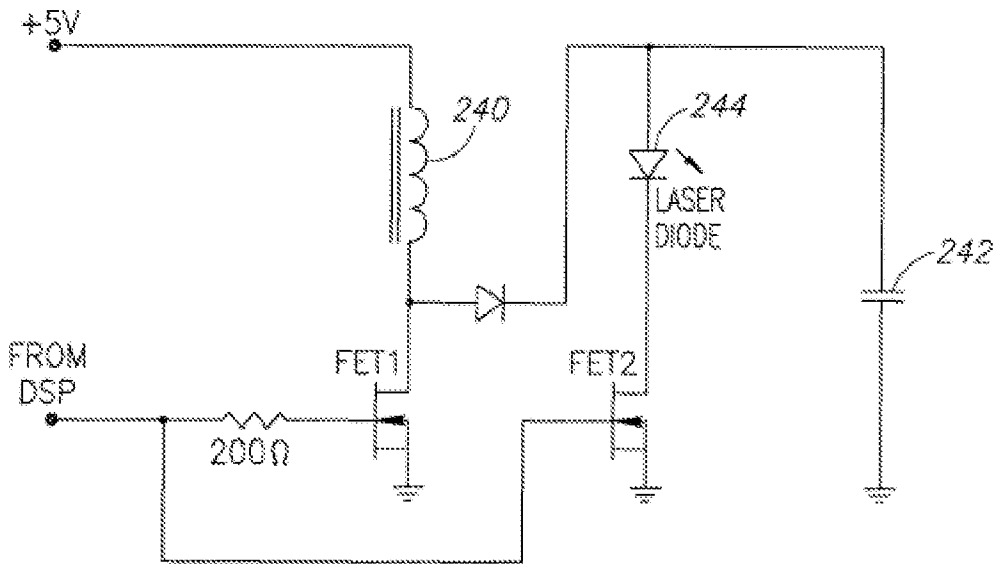
In view of the forgoing, Examiners find two possible interpretations of the operation of FIGS. 23B and 24 of Hall. This finding is confirmed by Patent Owner's expert Mr. Wolfe in the Wolfe Expert Report provided in related litigation as discussed above.

For information only, Examiners agree with Patent Owner that operation (a) of FIG. 23B of Hall discussed above does not read on the pending and examined claims because the capacitor 242 does not charge "responsive to the transistor being turned off" as recited in the claims because of the overlapping and delayed activation of FET1 and FET2.

Nevertheless, Examiners cannot ignore the other "possible" interpretation of the operation of FIG. 23B of Hall as proposed by Patent Owner's own expert during litigation. This operation (b) is the basis for the rejections applying FIG. 23B below.

B. Rejections Applying FIG. 23B of Hall

Regarding claim 1, FIG. 23B of Hall discloses **an apparatus** (See Hall FIG. 23B, reprinted below)**, comprising:**



Hall FIG. 23B

a voltage source (See FIG. 23B above, note voltage source +5V);

an inductor coupled to the voltage source, wherein the inductor is configured to store energy in a magnetic field (See FIG. 23B above, note inductor 240);

a diode coupled to the voltage source via the inductor (See FIG. 23B, note diode shown but not identified coupled to inductor 240);

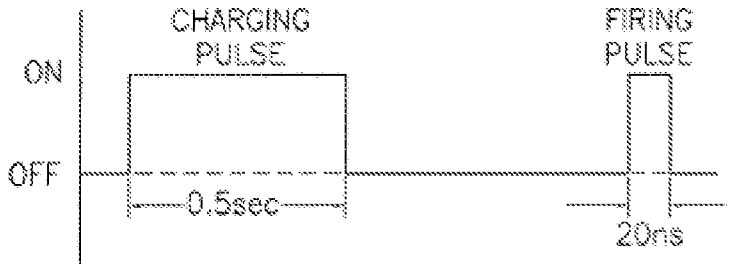
a transistor configured to be turned on and turned off by a control signal (See FIG. 23B, note transistor FET2 activated by DSP control signal);

a light emitting element coupled to the transistor (See FIG. 23B above, note laser diode 244);

a capacitor coupled to a charging path and a discharge path (See FIG. 23B, note capacitor 242. Note also Examiners' interpretation of charging path and the Patent Owner's interpretation of discharge path, specifically the path of charge moving at

discharge from the tope of capacitor 242 to ground)**, wherein the charging path includes the inductor and the diode, and wherein the discharge path includes the transistor and the light emitting element** (See FIG. 23B above, note charging path would include at least the inductor 240 and shown but not identified diode and discharge path would include at least the transistor FET2 and the laser diode 244. See also Hall col. 7, lines 42-46)**;**

wherein, responsive to the transistor being turned off, the capacitor charges via the charging path such that a voltage across the capacitor increases from a lower voltage level to a higher voltage level and the inductor is configured to release energy stored in the magnetic field such that a current through the inductor decreases from a higher current level to a lower current level (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above where in the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge. Finally note the inductor is “configured" as claimed)**; and**



Hall FIG. 24

wherein, responsive to the transistor being turned on, the capacitor is configured to discharge through the discharge path such that the light emitting element emits a pulse of light and the voltage across the capacitor decreases from the higher voltage level to the lower voltage level and the inductor is configured to store energy in the magnetic field such that the current through the inductor increases from the lower current level to the higher current level (See FIG. 23B, note configuration shown which provided the recited functionality. See also col. 7, lines 42-46. Specifically, when the transistor FET2 is on during the firing pulse, the capacitor is discharged so that the laser diode fires. Note also the inductor is "configured" as claimed).

Regarding claim 2, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the lower current level is approximately zero** (See FIG. 23B wherein energy stored in the inductor is transferred to the capacitor when the transistor is turned off. Thus, the energy remaining in the inductor would be "approximately zero").

Regarding claim 3, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the capacitor is charged immediately following emission of a pulse of light from the light emitting element** (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above where in the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge).

Regarding claim 4, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the higher voltage level is greater than a voltage of the voltage source** (See FIG. 23B above, note this is merely a property of the circuit shown)**, and wherein the diode has an anode coupled to the voltage source via the inductor and a cathode coupled to the capacitor, such that the diode is forward biased when the voltage across the capacitor is at the lower voltage level and the diode is reverse biased when the voltage across the capacitor is at the higher voltage level** (See FIG. 23B above, note shown but not identified diode coupled in series with the inductor 240).

Regarding claim 7, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the light emitting element is a laser diode** (See FIG. 23B above, note laser diode 244).

Regarding claim 9, FIG. 23B of Hall discloses **a method** (See FIG. 23B above and col. 7, lines 42-46 and FIG. 24)**, comprising:**

turning off a transistor (See col. 7, lines 42-47 wherein a transistor is turned on and off)**, wherein the transistor is coupled to a light emitting element** (See FIG. 23B above, note transistor FET2 coupled to laser diode 244)**, wherein both the transistor and the light emitting element are included in a discharge path coupled to a capacitor** (See FIG. 23B above. Note also Patent Owner's interpretation of discharge path as discussed above. Thus, note discharge path would include transistor FET2, capacitor 242 and laser diode 244)**, wherein the capacitor is also coupled to a charging path including a diode and an inductor, wherein the inductor is**

configured to store energy in a magnetic field, wherein the diode is coupled to a voltage source via the inductor (See FIG. 23B above. Note also Examiners' interpretation of charging path as discussed above. Thus, note charge path would include voltage source +5V, inductor 240 and series connected shown but not identified diode)**, and**

wherein, responsive to the transistor being turned off, the capacitor charges via the charging path such that a voltage across the capacitor increases from a lower voltage level to a higher voltage level and the inductor is configured to release energy stored in the magnetic field such that a current through the inductor decreases from a higher current level to a lower current level (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above where in the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge. Finally note the inductor is “configured" as claimed)**; and**

turning on the transistor, wherein responsive to the transistor being turned on, the capacitor discharges through the discharge path such that the light emitting element emits a pulse of light and the voltage across the capacitor decreases from the higher voltage level to the lower voltage level and the inductor is configured to store energy in the magnetic field such that the current through the inductor increases from the lower current level to the higher current

level (See FIG. 23B, note configuration shown which provided the recited functionality. See also col. 7, lines 42-46. Specifically, when the transistor FET2 is on during the firing pulse, the capacitor is discharged so that the laser diode fires. Note also the inductor is "configured" as claimed).

Regarding claim 10, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the lower current level is approximately zero** (See FIG. 23B wherein energy stored in the inductor is transferred to the capacitor when the transistor is turned off. Thus, the energy remaining in the inductor would be "approximately zero").

Regarding claim 11, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the capacitor is charged immediately following emission of a pulse of light from the light emitting element** (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above where in the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge).

Regarding claim 12, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the higher voltage level is greater than a voltage of the voltage source** (See FIG. 23B above, note this is merely a property of the circuit shown)**, and wherein the diode has an anode coupled to the voltage source via the inductor and a cathode coupled to the capacitor, such that the diode is forward biased when the voltage across the capacitor is at the lower voltage level and the diode is reverse**

biased when the voltage across the capacitor is at the higher voltage level (See FIG. 23B above, note shown but not identified diode coupled in series with the inductor 240).

Regarding claim 13, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the charging of the capacitor is carried out in about 500 nanoseconds** (Examiners find that this limitation is merely an intended result or property of the circuit and the turning on and off of the transistor in the method recited in claim 9. Accordingly, this limitation is non-limiting of the claim and thus FIG. 23B of Hall reads on this claim. Additionally and alternatively, since FIG. 23B of Hall otherwise discloses the recited circuit and performs the recited method steps, the circuit of Hall would be capable of meeting the intended result).

Regarding claim 14, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the light emitting element is a laser diode** (See FIG. 23B above, note laser diode 244).

Regarding claim 17, FIG. 23B of Hall discloses **a light detection and ranging (LIDAR) device** (See FIG. 23B above and FIG. 9A and see col. 3, lines 3-4 and col. 4, lines 41-43) **comprising:**

a light source including:

a voltage source (See FIG. 23B above, note voltage source +5V)**;**

an inductor coupled to the voltage source, wherein the inductor is configured to store energy in a magnetic field (See FIG. 23B above, note inductor 240)**;**

a diode coupled to the voltage source via the inductor (See FIG. 23B, note diode shown but not identified coupled to inductor 240);

a transistor configured to be turned on and turned off by a control signal (See FIG. 23B, note transistor FET2 activated by DSP control signal);

a light emitting element coupled to the transistor (See FIG. 23B above, note laser diode 244);

a capacitor coupled to a charging path and a discharge path (See FIG. 23B, note capacitor 242. Note also Examiners' interpretation of charging path and the Patent Owner's interpretation of discharge path, specifically the path of charge moving at discharge from the tope of capacitor 242 to ground), **wherein the charging path includes the inductor and the diode, and wherein the discharge path includes the transistor and the light emitting element** (See FIG. 23B above, note charging path which would include inductor 240 and shown but not identified diode and discharge path including the transistor FET2 and the laser diode 244. See also Hall col. 7, lines 42-46);

wherein, responsive to the transistor being turned off, the capacitor charges via the charging path such that a voltage across the capacitor increases from a lower voltage level to a higher voltage level and the inductor is configured to release energy stored in the magnetic field such that a current through the inductor decreases from a higher current level to a lower current level (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above where in the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are

off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge. Finally note the inductor is “configured" as claimed)**; and**

wherein, responsive to the transistor being turned on, the capacitor discharges through the discharge path such that the light emitting element emits a pulse of light and the voltage across the capacitor decreases from the higher voltage level to the lower voltage level and the inductor is configured to store energy in the magnetic field such that the current through the inductor increases from the lower current level to the higher current level (See FIG. 23B, note configuration shown which provided the recited functionality. See also col. 7, lines 42-46. Specifically, when the transistor FET2 is on during the firing pulse, the capacitor is discharged so that the laser diode fires. Note also the inductor is "configured" as claimed)**;**

a light sensor configured to detect a reflected light signal comprising light from the emitted light pulse reflected by a reflective object (See col. 3, lines 4-9 and col. 4, lines 21-26 wherein the circuit of FIG. 23B is part of a LIDAR system which uses photo detectors as light sensors as part of the system)**; and**

a controller configured to determine a distance to the reflective object based on the reflected light signal (See col. 4, lines 21-43 which uses a DSP to determine ranging information).

Regarding claim 18, FIG. 23B of Hall discloses the device of claim 17 and further wherein **the lower current level is approximately zero** (See FIG. 23B wherein energy

stored in the inductor is transferred to the capacitor when the transistor is turned off. Thus, the energy remaining in the inductor would be "approximately zero").

Regarding claim 19, FIG. 23B of Hall discloses the device of claim 17 and further wherein **the capacitor is charged immediately following emission of a pulse of light from the light emitting element** (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above where in the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge).

Regarding claim 21, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the discharge path forms a current path beginning at the first terminal of the capacitor and ending at ground** (See FIG. 23B above which shows the recited structures. Specifically note also Patent Owner's interpretation of discharge path being the path of charge/current from the capacitor to the ground which is shown in FIG. 23B).

Regarding claim 22, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the transistor and the light emitting element are coupled in series between the first terminal of the capacitor and ground** (See FIG. 23B above which shows the recited structures. Specifically note transistor FET2 and the laser diode 244 are coupled in series between the top plate of the capacitor 242 and the ground).

Regarding claim 23, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **an anode of the light emitting element is coupled to the capacitor** (See FIG. 23B above, note anode of laser diode 244 is coupled to the capacitor 242).

Regarding claim 24, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **a cathode of the light emitting element is coupled to the transistor** (See FIG. 23B above, note cathode of laser diode 244 is coupled to the transistor FET2).

Regarding claim 25, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the light emitting element is coupled between the capacitor and the transistor** (See FIG. 23B above, note laser diode 244 is coupled between the capacitor 242 and the transistor FET2).

Regarding claim 26, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **responsive to turning the transistor off, the capacitor charges to a voltage level equal to or greater than a voltage of the voltage source** (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge. Additionally, over time and after the charging pulse, the capacitor 242 will eventually be charge to a voltage level equal or greater than a voltage of the voltage source).

Regarding claim 27, FIG. 23B of Hall discloses the apparatus of claim 1 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the capacitor discharges and charges, respectively** (See FIG. 23B above and FIGS. 9A and 9B, note DSP as DSP sends control signals to transistors via laser/gate drivers. Further note operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Thus, during the pulse cycle shown in FIG. 24 above, FET2 will be turned on and off only once each time the capacitor is charged and discharged).

Regarding claim 28, FIG. 23B of Hall discloses the apparatus of claim 1 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the light emitting element emits the pulse of light** (See FIG. 23B above and FIGS. 9A and 9B, note DSP as DSP sends control signals to transistors via laser/gate drivers. Further note operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Thus, during the pulse cycle shown in FIG. 24 above, FET2 will be turned on and off only once during time the laser diode 244 emits light).

Regarding claim 30, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **the capacitor charges in response to turning off the transistor and**

only in response to turning off the transistor (See FIG. 23B above and operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Furthermore, as discussed above, following or in response to the FET2 turning off at the end of the firing pulse, the capacitor 242 will begin to charge and will continue charge during the time FET2 is off).

Regarding claim 31, FIG. 23B of Hall discloses the apparatus of claim 1 and further wherein **a first terminal of the capacitor is coupled to the discharge path and a second terminal of the capacitor is coupled to ground** (See FIG. 23B above, note first terminal of the capacitor 242 is coupled to the discharge path to ground through the laser diode 24 and FET2 and the second terminal of the capacitor 242 is connected directly to ground).

Regarding claim 33, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the discharge path forms a current path beginning at the first terminal of the capacitor and ending at ground** (See FIG. 23B above which shows the recited structures. Specifically note also Patent Owner's interpretation of discharge path being the path of charge/current from the capacitor to the ground which is shown in FIG. 23B).

Regarding claim 34, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the transistor and the light emitting element are coupled in series between the first terminal of the capacitor and ground** (See FIG. 23B above which shows the recited

structures. Specifically note the transistor FET2 and the laser diode 244 are coupled in series between the top plate of the capacitor 242 and ground).

Regarding claim 35, FIG. 23B of Hall discloses the method of claim 9 and further wherein **an anode of the light emitting element is coupled to the capacitor** (See FIG. 23B above, note anode of laser diode 244 is coupled to the capacitor 242).

Regarding claim 36, FIG. 23B of Hall discloses the method of claim 9 and further wherein **a cathode of the light emitting element is coupled to the transistor** (See FIG. 23B above, note cathode of laser diode 244 is coupled to the transistor FET2).

Regarding claim 37, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the light emitting element is coupled between the capacitor and the transistor** (See FIG. 23B above, note laser diode 244 is coupled between the capacitor 242 and the transistor FET2).

Regarding claim 38, FIG. 23B of Hall discloses the method of claim 9 and further wherein **responsive to turning the transistor off, the capacitor charges to a voltage level equal to or greater than a voltage of the voltage source** (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge. Additionally, over time and after the charging pulse, the

capacitor 242 will eventually be charge to a voltage level equal or greater than a voltage of the voltage source).

Regarding claim 39, FIG. 23B of Hall discloses the method of claim 9 and further wherein **turning on the transistor and turning off the transistor is performed once and only once each time the capacitor discharges and charges, respectively** (See FIG. 23B above and FIGS. 9A and 9B, note DSP as DSP sends control signals to transistors via laser/gate drivers. Further note operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Thus, during the pulse cycle shown in FIG. 24 above, FET2 will be turned on and off only once each time the capacitor is charged and discharged).

Regarding claim 40, FIG. 23B of Hall discloses the method of claim 9 and further wherein **turning on the transistor and turning off the transistor is performed once and only once each time the light emitting element emits the pulse of light** (See FIG. 23B above and FIGS. 9A and 9B, note DSP as DSP sends control signals to transistors via laser/gate drivers. Further note operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Thus, during the pulse cycle shown in FIG. 24 above, FET2 will be turned on and off only once during time the laser diode 244 emits light).

Regarding claim 42, FIG. 23B of Hall discloses the method of claim 9 and further wherein **the capacitor charges in response to turning off the transistor and only in**

response to turning off the transistor (See FIG. 23B above and operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Furthermore, as discussed above, following or in response to the FET2 turning off at the end of the firing pulse, the capacitor 242 will begin to charge and will continue charge during the time FET2 is off).

Regarding claim 43, FIG. 23B of Hall discloses the method of claim 9 and further wherein **a first terminal of the capacitor is coupled to the discharge path and a second terminal of the capacitor is coupled to ground** (See FIG. 23B above, note first terminal of the capacitor 242 is coupled to the discharge path to ground through the laser diode 24 and FET2 and the second terminal of the capacitor 242 is connected directly to ground).

Regarding claim 45, FIG. 23B of Hall discloses the device of claim 17 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the discharge path forms a current path beginning at the first terminal of the capacitor and ending at ground** (See FIG. 23B above which shows the recited structures. Specifically note also Patent Owner's interpretation of discharge path being the path of charge/current from the capacitor to the ground which is shown in FIG. 23B).

Regarding claim 46, FIG. 23B of Hall discloses the device of claim 17 and further wherein **the capacitor has a first terminal and a second terminal, and wherein the transistor and the light emitting element are coupled in series between the first terminal of the capacitor and ground** (See FIG. 23B above which shows the recited

structures. Specifically note the transistor FET2 and the laser diode 244 are connected in series between the top plate of the capacitor 242 and ground).

Regarding claim 47, FIG. 23B of Hall discloses the device of claim 17 and further wherein **an anode of the light emitting element is coupled to the capacitor** (See FIG. 23B above, note anode of laser diode 244 is coupled to the capacitor 242).

Regarding claim 48, FIG. 23B of Hall discloses the device of claim 17 and further wherein **a cathode of the light emitting element is coupled to the transistor** (See FIG. 23B above, note cathode of laser diode 244 is coupled to the transistor FET2).

Regarding claim 49, FIG. 23B of Hall discloses the device of claim 17 and further wherein **the light emitting element is coupled between the capacitor and the transistor** (See FIG. 23B above, note laser diode 244 is coupled between the capacitor 242 and the transistor FET2).

Regarding claim 50, FIG. 23B of Hall discloses the device of claim 17 and further wherein **responsive to turning the transistor off, the capacitor charges to a voltage level equal to or greater than a voltage of the voltage source** (See FIG. 23B above and FIG. 24, reprinted below. Note also operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 activated during the charging pulse and FET2 activates during the firing pulse. Further note that when both FETs are off following the firing pulse, the capacitor will charge. Thus, following or in response to FET2 turning off at the end of the firing pulse, both FETs will be off and the capacitor 242 will begin to charge. Additionally, over time and after the charging pulse, the

capacitor 242 will eventually be charge to a voltage level equal or greater than a voltage of the voltage source).

Regarding claim 51, FIG. 23B of Hall discloses the device of claim 17 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the capacitor discharges and charges, respectively** (See FIG. 23B above and FIGS. 9A and 9B, note DSP as DSP sends control signals to transistors via laser/gate drivers. Further note operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Thus, during the pulse cycle shown in FIG. 24 above, FET2 will be turned on and off only once each time the capacitor is charged and discharged).

Regarding claim 52, FIG. 23B of Hall discloses the device of claim 17 and further comprising **a gate driver to provide the control signal to turn on and off the transistor, wherein the gate driver provides the control signal to turn the transistor on and off once and only once each time the light emitting element emits the pulse of light** (See FIG. 23B above and FIGS. 9A and 9B, note DSP as DSP sends control signals to transistors via laser/gate drivers. Further note operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Thus, during the pulse cycle shown in FIG. 24 above, FET2 will be turned on and off only once during time the laser diode 244 emits light).

Regarding claim 54, FIG. 23B of Hall discloses the device of claim 17 and further wherein **the capacitor charges in response to turning off the transistor and only in response to turning off the transistor** (See FIG. 23B above and operation (b) discussed above wherein the FETs are activated independently, i.e., FET1 is activated during the charging pulse and FET2 is activated during the firing pulse. Furthermore, as discussed above, following or in response to the FET2 turning off at the end of the firing pulse, the capacitor 242 will begin to charge and will continue charge during the time FET2 is off).

Regarding claim 55, FIG. 23B of Hall discloses the device of claim 17 and further wherein **a first terminal of the capacitor is coupled to the discharge path and a second terminal of the capacitor is coupled to ground** (See FIG. 23B above, note first terminal of the capacitor 242 is coupled to the discharge path to ground through the laser diode 24 and FET2 and the second terminal of the capacitor 242 is connected directly to ground).

Obviousness Rejections Applying FIG. 23B of Hall and Liero

Claims 5, 6, 16 and 20 are rejected under 35 U.S.C. 103 as being unpatentable over FIG. 23B of Hall in view of Liero. Examiners find that Liero is proper in this reexamination proceeding because it is a printed publication. (See MPEP §2210 and §2244--SNQs must be based on patents and printed publications). Examiners further find that Liero was published in IEEE as part of the IEEE MTT-S International Symposium in May 2010.

Regarding claim 5, FIG. 23B of Hall teaches the device of claim 1 and further the use of a field effect transistor, but not the specific type thereof. Nevertheless, Liero teaches the use of **gallium nitride field effect transistors (GaNFET)** for various applications. (See Liero Part I, Introduction). It would have been obvious at the time of the effective filing date to use GaNFETs for the transistors in the apparatus of FIG. 23B of Hall. One having ordinary skill in the art would make such a combination to provide a transistor that is an "ideal candidate ... for applications, where fast switching of high current is needed." (See Liero at least Part I, Introduction). Furthermore, the example of the application where such "fast switching" is needed to which to apply the GaNFET as taught by Liero is a diode laser circuit. (See Liero Parts I, II and IV wherein the GaNFET is used as the switching transistor for the diode laser circuit).

Regarding claim 6, FIG. 23B of Hall and Liero teach the apparatus of claim 5 and further wherein **the control signal applies voltage to a gate of the GaNFET to selectively turn the GaNFET on and off** (Note combination proposed for claim 5. See also Hall FIG. 23B above wherein the control signal is supplied to the gate of the transistor 200 which would be a GaNFET in view of the combination).

Regarding claim 16, FIG. 23B of Hall teaches the method of claim 9 and further wherein **the transistor is turned on and turned off by applying a control signal to a gate of the transistor** (See FIG. 23B above, note control signal to transistor 200), but not specifically the transistor being a GaNFET transistor. Nevertheless, Liero teaches the use of **gallium nitride field effect transistors (GaNFET)** for various applications. (See Liero Part I, Introduction). It would have been obvious at the time of the effective

filing date to use GaNFETs for the transistors in the apparatus of FIG. 23B of Hall. One having ordinary skill in the art would make such a combination to provide a transistor that is an "ideal candidate ... for applications, where fast switching of high current is needed." (See Liero at least Part I, Introduction). Furthermore, the example of the application where such "fast switching" is needed to which to apply the GaNFET as taught by Liero is a diode laser circuit. (See Liero Parts I, II and IV wherein the GaNFET is used as the switching transistor for the diode laser circuit).

Regarding claim 20, FIG. 23B of Hall teaches the device of claim 17 and further the use of a field effect transistor, but not the specific type thereof. Nevertheless, Liero teaches the use of **gallium nitride field effect transistors (GaNFET)** for various applications. (See Liero Part I, Introduction). It would have been obvious at the time of the effective filing date to use GaNFETs for the transistors in the apparatus of FIG. 23B of Hall. One having ordinary skill in the art would make such a combination to provide a transistor that is an "ideal candidate ... for applications, where fast switching of high current is needed." (See Liero at least Part I, Introduction). Furthermore, the example of the application where such "fast switching" is needed to which to apply the GaNFET as taught by Liero is a diode laser circuit. (See Liero Parts I, II and IV wherein the GaNFET is used as the switching transistor for the diode laser circuit).

Obviousness Rejection Applying FIG. 23B of Hall

Claim 13 is rejected under 35 U.S.C. §103 as being unpatentable over FIG. 23B of Hall. See MPEP §2112(III-IV) allowing alternative rejections under 35 U.S.C. §102

and §103 when there is a question of inherency of whether a prior art device is capable of meeting an intended result or property of the claim. As discussed above, Examiners find that wherein the charging of the capacitor is carried out in about 500 nanoseconds is merely an intended result or property of the claimed circuit and method. Nevertheless, even if it is assumed FIG. 23B of Hall does not explicitly disclose or teach such a feature, such charging would be obvious to one having ordinary skill in the art.

Examiners first find that FIG. 23B of Hall otherwise discloses each and every feature of claim 13 and further providing a charging pulse to the capacitor of 5000 nanoseconds, but not explicitly a "charging" of the capacitor in about 500 nanoseconds. Nevertheless, modifying or operating FIG. 23B of Hall to have the relative charging time as recited in the claims would be obvious to one having ordinary skill in the art through routine experimentation because where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation and the claimed device is not patentably distinct from the prior art device. See MPEP §2144.05(ii). It would have thus have been obvious to optimize the charging time of the capacitor in FIG. 23B of Hall to be about 500 nanoseconds because such optimization would be routine skill in the art to maximize the performance of the known circuit structures shown in FIG. 23B of Hall, i.e., optimization of the capacitor structure and the timing of the firing of the transistor.

IX. CONFIRMED/PATENTABLE CLAIMS

Claims 32, 44 and 56 are found patentable herein. While Examiners find that the prior art cited in the Request, particularly Hall and Renz discloses each and every feature of claims 1, 9 and 17 from which these claims depend, Examiners find the prior art cited in the Request does not disclose or teach coupling a second terminal of the capacitor to a reference voltage other than ground as recited in these claims and in combination with the other features of these claims.

X. EXAMINERS' RESPONSES TO PATENT OWNER'S ARGUMENTS

Regarding the Patent Owner's comments and arguments with respect to the interpretation of discharge path (See May 2018 Amendment pp. 28-33), Examiners note those comments were addressed in the Claim Interpretation section above.

Regarding the Patent Owner's comments and arguments with respect to the operation of FIG. 23B of Hall (See May 2018 Amendment pp. 13-16 and 24-25), Examiners note those comments were address in the body of the anticipation rejection applying FIG. 23B of Hall.

Examiners further note that the rejections applying Renz have been withdrawn herein and thus arguments directed to those rejections are generally moot herein.

A. Comparison of Circuits

Regarding the Patent Owner's discussion provided at pages 19-28 of the May 2018 Amendment, Examiners find Patent Owner is comparing the circuit disclosed in the 936 Patent to the circuits in Renz and Hall. Examiners do not disagree that the

topography of the specific circuit shown in FIG. 5A of the 936 Patent is different from the specific circuits shown in each of Renz and Hall and thus the operation of these specific circuits would be different in one or more ways. Nevertheless, Examiners note it is the claims that are issue here. As found above and not disputed by Patent Owner, Examiners find no lexicographic definitions in the 936 Patent specification, no claim invoke interpretation under 35 U.S.C. §112 (6th ¶) and further no disclaimers are present in the 936 Patent specification. Accordingly, the claims will be given their broadest reasonable interpretation. Examiners further note it is improper to import claim limitations from the specification, i.e., a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment. See MPEP §2111.01(II). Finally, Examiners find the 936 Patent specification explicitly states the "various example aspects and example embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims" (See 936 Patent at col. 27, line 66-col. 28, line 3). Accordingly, under the broadest reasonable interpretation, Examiners cannot import claim limitations from the specification since the claims are broader than any embodiment in the specification. Furthermore, the specification of the 936 Patent explicitly directs examiners to not import any limitations from the specification to the claims. Therefore, while Examiners recognize the specific circuit shown in the figures of the 936 Patent, such circuit is not controlling or helpful in distinguishing the prior art. Rather it is only appropriate to consider the claim language as limiting the claim language.

B. Rejections Applying FIG. 23A of Hall

Regarding the rejections applying FIG. 23A of Hall, Patent Owner attempts to differentiate the claims on the basis of Patent Owner's interpretation of discharge path. Specifically, Patent Owner argues that "[n]either the circuits in Hall nor Renz relied on discloses a light emitting element included with the transistor in the discharge path." See May 2018 Amendment page 34. Examiners disagree. As discussed above, Examiners' interpretation of discharge path include both the path of charge from the capacitor to the ground as well as the path of charge from ground to the capacitor during discharge of the capacitor. On this basis Examiners find that FIG. 23A of Hall reads on the claims.

Furthermore, Patent Owner's arguments and the specification of the 936 Patent are helpful in this analysis. For example, Patent Owner attempts to distinguish FIG. 23A of Hall on the basis that light emitting elements and the transistors are not in "the discharge current path." See May 2018 Amendment page 34. Thus, if Patent Owner's interpretation of "discharge path" is so clear and well defined, why is Patent Owner using another phrase for support and argument? It does not make sense that Patent Owner is on one hand trying to state the interpretation of discharge path is so well known and clear but on the other hand is not even using this phrase to differentiate the prior art by using another phrase ("discharge current path").

In view of the forgoing and on the basis of Examiners' interpretation of discharge patent, the rejections applying FIG. 23A of Hall are maintained herein.

C. Rejections Applying FIG. 23B of Hall

Regarding the rejections applying FIG. 23B of Hall, Patent Owner argues that operation (a) of FIG. 23B of Hall (discussed above in the rejection) controls and that the capacitor 242 does not charge in response to turning off FET2. While Examiners agree that operation (a) of FIG. 23B of Hall would not read on the claims, such a finding does not overcome the rejection because Examiners nevertheless find that operation (b) of FIG. 23B of Hall does read on the claims. Operation (b) of FIG. 23B of Hall is the basis for the rejections as provided above.

While Examiners have fully considered Patent Owner's arguments in the May 2018 Amendment and the May 2018 Wolfe Declaration, Examiners cannot ignore the Wolfe Expert Report made by the same Patent Owner and same expert in prior litigation. As discussed above in the FIG. 23B of Hall rejections, Examiners find that Mr. Wolfe in the Wolfe Expert Report stated that there were two possible interpretations of FIG. 23B of Hall, i.e., operation (a) and operation (b). Thus, Examiners find it reasonable to apply either interpretation for purposes of rejection herein.

Examiners further recognize the change in position of both the Patent Owner and Mr. Wolfe from the two possible interpretations of FIG. 23B of Hall during related litigation to only one now (operation (a)) during reexamination in an attempt to overcome the rejections. However, Examiners find that Patent Owner has not made any attempt to discount or discredit these two possible interpretations (specifically operation (b)) made in the related litigation. Accordingly, Examiners find the rejections applying FIG. 23B of Hall using operation (b) reasonable and the rejections are maintained.

D. Dependent Claims

Patent Owner makes general arguments asserting that the newly added/amended dependent claims 21-56 overcome either FIG. 23A or FIG. 23B of Hall. Examiners disagree for claims 21-31, 33-43 and 45-55 as they are all rejected as provided above. Nevertheless, Examiners agree that claims 32, 44 and 56 are allowable over Renz or Hall and thus these claims are allowed.

XI. LITIGATION IN RELATION TO U.S. PATENT NO. 9,368,936

It is noted that pending litigation was found regarding the 936 Patent, *Waymo LLC v. Ulber Technologies, Inc. et al.*, 3:17cv939 (U.S. Dist. Cal. Northern). However, Examiners find it appears from the record for this litigation that the patent claims were dismissed on July 7, 2017. Nevertheless, the patent owner is reminded of the continuing responsibility under 37 C.F.R. §1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§2207, 2282 and 2286.

XII. CONCLUDING REMARKS

Claims 1-56 are subject to reexamination herein.

Claims 1-31, 33-43 and 45-55 are rejected herein.

Claims 32, 44 and 56 are found patentable.

THIS ACTION IS MADE FINAL.

A shortened statutory period for response to this action is set to expire two months from the mailing date of this action. Patent Owner's amendments to the claims provided in the May 2018 Amendment necessitated the new/amended grounds of rejection herein.

Extensions of time under 37 C.F.R. §1.136(a) do not apply in reexamination proceedings. The provisions of 37 C.F.R. §1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Further, in 35 U.S.C. §305 and in 37 C.F.R. §1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."

Extensions of time in reexamination proceedings are provided for in 37 C.F.R. §1.550(c). A request for extension of time must specify the requested period of extension and it must be accompanied by the petition fee set forth in 37 C.F.R. §1.17(g). Any request for an extension in a third party requested ex parte reexamination must be filed on or before the day on which action by the patent owner is due, and the mere filing of a request will not effect any extension of time. A request for an extension of time in a third party requested ex parte reexamination will be granted only for sufficient cause, and for a reasonable time specified. Any request for extension in a patent owner requested ex parte reexamination (including reexamination ordered under 35 U.S.C. §257) for up to two months from the time period set in the Office action must be filed no later than two months from the expiration of the time period set in the Office action. A request for an extension in a patent owner requested ex parte

reexamination for more than two months from the time period set in the Office action must be filed on or before the day on which action by the patent owner is due, and the mere filing of a request for an extension for more than two months will not effect the extension. The time for taking action in a patent owner requested ex parte reexamination will not be extended for more than two months from the time period set in the Office action in the absence of sufficient cause or for more than a reasonable time.

The filing of a timely first response to this final rejection will be construed as including a request to extend the shortened statutory period for an additional two months. In no event, however, will the statutory period for response expire later than SIX MONTHS from the mailing date of the final action. See MPEP § 2265.

All correspondence relating to this ex parte reexamination proceeding should be directed as follows:

By U.S. Postal Service Mail to:

Mail Stop Ex Parte Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By hand to:

Customer Service Window Randolph Building
401 Dulany St.
Alexandria, VA 22314

For EFS-Web transmissions, 37 C.F.R. §1.8(a)(1)(i) (C) and (ii) states that correspondence (except for a request for reexamination and a corrected or replacement request for reexamination) will be considered timely filed if (a) it is transmitted via the

Office's electronic filing system in accordance with 37 C.F.R. §1.6(a)(4), and (b) includes a certificate of transmission for each piece of correspondence stating the date of transmission, which is prior to the expiration of the set period of time in the Office action. Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

/KENNETH J WHITTINGTON/
Primary Examiner, Art Unit 3992

Conferees:
/My Trang Ton/
Primary Examiner, Art Unit 3992

/NICK CORSARO/
Acting SPE, Art Unit 3992